KFLOP DIGITAL I/O **Bottom Left Of Kflop Board** setbit16 =1 is off; clearbit16 is on

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	KFLOP	Kflop JP4 AUX Connector 0	1	VDD5	+5 Volts Output	DO NOT USE	
	Digital I/O		2	VDD12	+12 Volts Output	DO NOT USE	
			3	VDD33	+3.3 Volts Output		P2 on opto board
			4	RESET#	Power up Reset (low true) output		
	16		5	IO-16	Gen Purpose LVTTL I/O (3.3V Only)	Spindle CW M3	216
	17		6	IO-17	Gen Purpose LVTTL I/O (3.3V Only)	Spindle CCW M4	220
	18		7	IO-18	Gen Purpose LVTTL I/O (3.3V Only)	Spindle Stop M5	222
			8	GND	Digital Ground		
			9	GND	Digital Ground		
	19		10	IO-19	Gen Purpose LVTTL I/O (3.3V Only)	Control E-Stop	244 10CRE
	20		11	IO-20	Gen Purpose LVTTL I/O (3.3V Only)	Drive Enable	245 11CRE
	21		12	IO-21	Gen Purpose LVTTL I/O (3.3V Only)	E-Stop Reset	274
	22		13	IO-22	Gen Purpose LVTTL I/O (3.3V Only)	Cycle Start Lamp	246
	23		14	IO-23	Gen Purpose LVTTL I/O (3.3V Only)	Manual Mode	294 16CRE
	24		15	IO-24	Gen Purpose LVTTL I/O (3.3V Only)	Low Range Lamp	271 15CRE
	25		16	IO-25	Gen Purpose LVTTL I/O (3.3V Only)	High Range lamp	270

KFLOP DIGITAL I/O **Bottom Center of Kflop Board**

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	KFLOP	Kflop JP6 AUX Connector 1	1	VDD5	+5 Volts Output	DO NOT USE	
	Digital I/O		2	VDD12	+12 Volts Output	DO NOT USE	
			3	VDD33	+3.3 Volts Output		
			4	RESET#	Power up Reset (low true) output		
	26		5	26	Gen Purpose LVTTL I/O (3.3V Only)		
	27		6	27	Gen Purpose LVTTL I/O (3.3V Only)		
	28		7	28	Gen Purpose LVTTL I/O (3.3V Only)		
			8	GND	Digital Ground		
			9	GND	Digital Ground		
	29		10	29	Gen Purpose LVTTL I/O (3.3V Only)		
	30		11	30	Gen Purpose LVTTL I/O (3.3V Only)		
	31		12	31	Gen Purpose LVTTL I/O (3.3V Only)		
	32		13	32	Gen Purpose LVTTL I/O (3.3V Only)		
	33		14	33	Gen Purpose LVTTL I/O (3.3V Only)		
	34		15	34	Gen Purpose LVTTL I/O (3.3V Only)		
	35		16	35	Gen Purpose LVTTL I/O (3.3V Only)		

KANALOG BOARD

KFLOP DIGITAL I/O — **Top of Kanalog Board on Left**

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	Digital I/O KFLOP 0	Kanalog JP1 Diff. Inputs	1	0		Encoder X Ch A+	X Axis Table
			2	0		Encoder X Ch A-	
	KFLOP 1		3	1		Encoder X Ch B+	
			4	1		Encoder X Ch B-	
	KFLOP 2		5	2		Encoder Y Ch A+	Y Axis Saddle
			6	2		Encoder Y Ch A-	
	KFLOP 3		7	3		Encoder Y Ch B+	
			8	3		Encoder Y Ch B-	
	KFLOP 4		9	4		Encoder Z Ch A+	Z Axis Quill
			10	4		Encoder Z Ch A-	
	KFLOP 5		11	5		Encoder Z Ch B+	
			12	5		Encoder X Ch B-	
	KFLOP 6		13	6		Encoder A Ch A+	A Axis 4th Axis
			14	6		Encoder A Ch A-	
	KFLOP 7		15	7		Encoder A Ch B+	
			16	7		Encoder A Ch B-	

KFLOP DIGITAL I/O — **Top of Kanalog Board on Right**

	Digital I/O KFLOP 36	Kanalog JP2 Diff. Inputs	1	36		Encoder X Index+	Encoder Index
			2	36		Encoder X Index-	
	KFLOP 37		3	37		Encoder Y Index+	
			4	37		Encoder Y Index-	
	KFLOP 38		5	38		Encoder Z Index+	
			6	38		Encoder Z Index-	
	KFLOP 39		7	39		Encoder A Index+	
			8	39		Encoder A Index-	
	KFLOP 40		9	40			
			10	40			
	KFLOP 41		11	41			
			12	41			
	KFLOP 42		13	42			
			14	42			
	KFLOP 43		15	43			
			16	43			

KANALOG ANALOG I/O **Upper Left Of Kanalog Board**

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	ADC 0	Kanalog JP6 Analog In +/- 10V	0	Kanalog Analog I/O			
	ADC 1		1	ADC Inputs 0-7			
	ADC 2		2		2048 = +10v		
	ADC 3		3		-2048 = -10v		
	ADC 4		4				
	ADC 5		5				
	ADC 6		6				
	ADC 7		7				
			Gnd				
			Gnd				
			Gnd				
			Gnd				
			Gnd				
			Gnd				
			Gnd				
			Gnd				

KANALOG DIGITAL I/O **Upper Right Of Kanalog Board**

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	152	Kanalog JP8 FET Relay Drivers	SW0	SW0	active when checked or with state=1		
	153		SW1	SW1			
	154		SW2	SW2			
	155		SW3	SW3			
	156		SW4	SW4			
	157		SW5	SW5			
	158		SW6	SW6			
	159		SW7	SW7			
			SWE	SWE	Watchdog - Switch Enable All		
			3.3V	3.3V	+3.3V low current (<100ma)		
			3.3V	3.3V			
			1.7V	1.7V	Low current 1.7V bias current		
			+5V	+5V	5V sourced from white molex connector		
			+5V	+5V			
			+5V	+5V			
			+5V	+5V			

KANALOG ANALOG I/O **Lower Left Of Kanalog Board**

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	DAC 0	Kanalog JP11 Analog Out +/- 10V	0	DAC 0		X Gettys controller	X Axis +
	DAC 1		1	DAC 1		Y Gettys Controller	Y Axis +
	DAC 2		2	DAC 2		Z Gettys Controller	Z Axis +
	DAC 3		3	DAC 3		A	A Axis +
	DAC 4		4	DAC 4		Spindle RPM	Spindle RPM+
	DAC 5		5	DAC 5			
	DAC 6		6	DAC 6			
	DAC 7		7	DAC 7			
			Gnd			X Gettys controller	X Axis -
			Gnd			Y Gettys Controller	Y Axis -
			Gnd			Z Gettys Controller	Z Axis -
			Gnd			A	A Axis -
			Gnd			Spindle RPM	Spindle RPM-
			Gnd				
			Gnd				
			Gnd				

KANALOG DIGITAL I/O **Bottom Of Kanalog Board on Left**

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	144	Kanalog JP13 Opto Outputs	0+				
			0-				
	145		1+				
			1-				
	146		2+				
			2-				
	147		3+				
			3-				
	148		4+				
			4-				
	149		5+				
			5-				
	150		6+				
			6-				
	151		7+				
			7-				

KANALOG DIGITAL I/O **Bottom Of Kanalog Board on Right**

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	136	Kanalog JP15 5-24V Opto Inputs	0+				X, Y, Z, Knee Limits
			0-				
	137		1+				X Home
			1-				
	138		2+				Y Home
			2-				
	139		3+				Z Home
			3-				
	140		4+				A Home
			4-				
	141		5+				
			5-				
	142		6+				
			6-				
	143		7+				
			7-				

KANALOG DIGITAL I/O **Ribbon On Lower Right of Kanalog Board** 40 pin IDC header

Mach3	Bit #	Board	Pin	I/O Name	Description	Signal Name	Comments
	128	Kanalog JP12 2x20 Ribbon	1	in 0	Kanalog input bits		
	129		2	in 1	Kanalog input bits		
	130		3	in 2	Kanalog input bits		
	131		4	in 3	Kanalog input bits		
	132		5	in 4	Kanalog input bits		
	133		6	in 5	Kanalog input bits		
	134		7	in 6	Kanalog input bits		
	135		8	in 7	Kanalog input bits		
	160		9	out 0	Kanalog output bits		
	161		10	out 1	Kanalog output bits		
	162		11	out 2	Kanalog output bits		
	163		12	out 3	Kanalog output bits		
	164		13	out 4	Kanalog output bits		
	165		14	out 5	Kanalog output bits		
	166		15	out 6	Kanalog output bits		
	167		16	out 7	Kanalog output bits		

		Kanalog JP12 2x20 Ribbon	17	IN 0	ADC Channel 0-3 V		
			18	IN 1	ADC Channel 0-3 V		
			19	IN 2	ADC Channel 0-3 V		
			20	IN 3	ADC Channel 0-3 V		
			21				
			22				
			23				
			24				
			25	V 15	+15V from internal DC-DC generator 70ma max		
			26				
			27	VM 15	-15V from internal DC-DC generator 70ma max		
			28		Switch Misc activates FET Gate (pin 30)		
			29		Enable All if a logic level is desired instead of using FET Switch		
			30		FET Misc Gate		
			31	VDD 3.3	+3.3 V regulated down from 5V		
			32	VDD 3.3	+3.3 V regulated down from 5V		
			33	VDD 5	+5 V output only		
			34	VDD 5	+5 V output only		
			35	VDD 5	+5 V output only		
			36	VDD 5	+5 V output only		
			37	GND	common ground		
			38	GND	common ground		
			39	GND	common ground		
			40	GND	common ground		